AP-~~~~BD
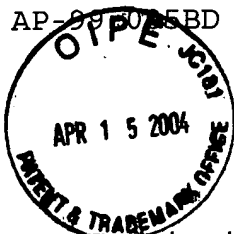
April 5, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile,   Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject:

| Serial No.   10/790,578   03/01/04 |

Peter Lee et al.

ARRAY ARCHITECTURE AND PROCESS FLOW
OF NONVOLATILE MEMORY DEVICES FOR
MASS STORAGE APPLICATIONS

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
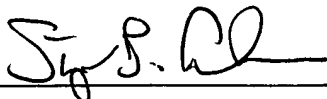
In An Application.

The following Patents and/or Publications are submitted to

comply with the duty of disclosure under CFR 1.97-1.99 and

37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on April 12, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date _____ 4/12/04

1

Atwood et al., "Intel Strata Flash TM Memory Technology Overview," Intel Technology Journal, 4th quarter 1997, pp.1-12, describes a stacked gate structure in which an ETOX process is used to produce a multiple level cell to store two bit in the same memory cell.

U.S. Patent 5,828,600 to Kato et al., "Non-Volatile Semiconductor Memory," describes a nonvolatile semiconductor memory where the cells are a MOSFET with a floating gate and have low power, high speed and reduced cell area.

U.S. Patent 5,095,344 to Harari, "Highly Compact EPROM and Flash EEPROM Devices," discloses a highly compact flash memory device using an intelligent programming technique to allow multiple bits to be stored in each cell and an intelligent erase program to extend the useful life of each cell.

U.S. Patent 5,029,130 to Yeh, "Single Transistor Non-Volatile Electrically Alterable Semiconductor Memory Device," discloses a single transistor electrically programmable and erasable memory cell using a split gate which allows the control gate to control a portion of the channel and the floating gate to control the remaining portion of the channel.

U.S. Patent 5,400,279 to Momodomi et al., "Nonvolatile Semiconductor Memory Device with NAND Cell Structure," discloses a nonvolatile memory device with a NAND cell structure.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449	Docket Number (Optional)	Application Number
INFORMATION DISCLOSURE CITATION IN AN APPLICATION	AP-99-005	10/790,578
	Applicant P. Lee et al.	
(use several sheets if necessary)	Filing Date 03/01/04	Group Art Unit

O | P ... APR 1 5 2004 (stamp)

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5828600	10/27/98	Kato et al.	365	185.11	10/30/96
	5400279	3/21/95	Momodomi et al.	365	185	5/26/93
	5095344	3/10/92	Harari	357	23.5	6/8/88
	5029130	7/2/91	Yeh	365	185	1/22/90

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

—	Atwood et al, "Intel Strata Flash TM Memory Technology Overview", Intel Technology Journal, 4th quarter 1997, pp. 1-12.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.